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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,093	11/21/2001	Jeffrey Binder	1303.65625	1287

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EXAMINER
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CHOWDHURY, SUMAIYA A

ART UNIT	PAPER NUMBER
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2623

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 09/990,093	Applicant(s) BINDER ET AL.	
	Examiner Sumaiya A. Chowdhury	Art Unit 2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 April 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 28-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 28-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some    \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/01/07 has been entered.

### *Response to Arguments*

2. Applicant's arguments with respect to claims 28-32 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 4/01/07 have been fully considered but they are not persuasive.

(a) Applicant argues "Independent claim 28 is distinguishable over Rege in that claim 28 recites a semiconductor memory array. In contrast, Rege shows disk memory in Fig. 2" on page 5, 3<sup>rd</sup> paragraph of the Remarks filed 4/01/07.

In reference to col.5, lines 37-46, Rege teaches the disk systems 800 are arranged as a hierarchy of redundant arrays of independent disk, e.g. a RAID type of storage device. Therefore, Rege teaches a memory array, but fails to teach a semiconductor memory array. Yamaguchi has <sup>been</sup> brought in to teach this limitation.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege in view of Rebec (5619528) and Yamaguchi (6342921).

As for claim 28, Rege teaches a system for distributing content comprising:

a memory array (redundant array 800) that stores content – col. 5, lines 37-45;

a first stream server module (first server 300) comprising;

a first stream server processor (cpu 310 – fig. 3) that requests content

(The processor within server 300 requests content from disk 800 - col. 3, lines 28-33);

a first media access controller (cpu 310) that receives the content and serializes the received content (The content is accessed sequentially – col. 6, lines 47-59); and

a first media interface module (321, 331, 341 – fig. 3) that formats the serialized content from the first media access controller into a format for a physical interface (The data is formatted according to the corresponding interface it is transmitted to. In other words, if it is transmitted to a WAN, it is formatted accordingly. - col. 3, lines 42-56);

a second stream server module (second server 300); and  
an interconnect (switch 400) connected to the memory and the first stream server module and the second stream server module (fig. 2; col. 3, line 64 – col. 4, line 9) comprising;

an address bus (Lines 401, 402, 403) coupled between first stream server module and the memory array and coupled between the second stream server module and semiconductor memory array that carries content addresses (Lines 401, 402, and 403 allow switching elements 500 to connect the servers 300 to the disks 800. The content along with its corresponding destination address is transmitted over lines 401, 402, and 403 – col. 3, line 64 – col. 4, line 15);

a data bus (Lines 401, 402, 403) coupled between first stream server module and the memory array and coupled between the second stream server module and the memory array that carries content (Lines 401, 402, and 403 allow switching elements 500 to connect the servers 300 to the disks 800. The content along with its corresponding destination address is transmitted over lines 401, 402, and 403 – col. 3, line 64 – col. 4, line 15); and

an arbitrator (600) that determines which of the first stream server module and the second stream server module may access either the address bus or the data bus based and which of the first stream server module and the second stream server module has priority (col. 3, lines 35-41, col. 3, line 64-col. 4, line 8, col. 5, line 10-18).

However, Rege fails to teach:

Semiconductor memory;

A server processor that encodes content;

A media access controller that receives encoded content;

In an analogous art, Rebec teaches a server processor (843F) that encodes content (col. 11, lines 30-37) and a media access controller (851F) that receives the encoded content (col. 11, lines 30-37);

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege's invention to include the above mentioned limitation, as taught by Rebec, for the well known advantage of converting the data for transmission.

However, Rege and Rebec fails to teach semiconductor memory.

In an analogous art, Yamaguchi teaches using semiconductor memory to store data such that the storage contents are held even if a power source is turned off and data can be electrically erased and rewritten in a lump every whole memory or every divided region.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege and Rebec's invention to include the above mentioned limitation, as taught by Yamaguchi, for the advantage of storing data such that the storage contents are held even if a power source is turned off and data can be electrically erased and rewritten in a lump every whole memory or every divided region.

Claim 29 contains the limitations of claim 28 and is analyzed as previously discussed with respect to that claim (In reference to fig. 2 in Rege, the second sever module (second server 300) is identical to the first server module (first sever 300). Therefore, the second server module contains the same elements and functions similarly to the first server module).

As for claim 30, Rege, Rebec, and Yamaguchi teach the claimed limitations. In particular, Rege teaches wherein the first stream server module further comprises:

a control processor that receives control packets that control how the content is output by the first stream server processor (The packet received by server 300 includes load information - col. 6, lines 30-55).

5. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege, Rebec, and Yamaguchi as applied to claim 28 above, and further in view of Kondo (7127736).

As for claim 31, Rege, Rebec, and Yamaguchi disclose the claimed limitations. In particular, Rege teaches wherein the first stream server processor further comprises:  
a first stream controller comprising:

an address generator that generates content addresses that are forwarded to the address bus (It is inherent for the processor of server 300 to generate content addresses which are forwarded to the address bus in switch 400, such that switch 400 can route the content to the appropriate disk 800. – col. 5, lines 24-30);

a payload data buffer that receives content from the data bus – (Since the requested content is buffered in cache 832, the content is sent as buffered data segments to the memory in server 300. Therefore, the memory in server 300 acts as a buffer. – col. 6, lines 30-39);

a control data buffer that receives control data (Control data received includes load information, server, switch and disk failures, rerouting information, priority information, or other positional information necessary. Col. 6, lines 42-46); and

Rebec teaches:

a protocol stream encoder/decoder (841S, 841F, 843S, 843F, 855FA, 855FB, 855SA, 855SB, 851F & 851S) for receiving content –col. 11, lines 30-61.

However, Rege and Rebec fail to teach an encoder/decoder for receiving control data from the control data buffer.

In an analogous art, Kondo teaches a decoder (27-fig. 2) which receives control data (index information) from the control data buffer (35 – fig. 2) – col. 11, lines 1-13, col. 11, line 60 – col. 12, line 15.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify Rege, Rebec, and Yamaguchi's invention to include the above mentioned limitation, as taught by Kondo, in order to receive information specifying particular scenes.

As for claim 32, Rege, Rebec, Yamaguchi, and Kondo disclose the claimed limitations. In particular, Rebec teaches wherein the protocol stream encoder/decoder further comprises:

at least two protocol encoder logic modules (855FA & FB, 855 SA & SB) that receives the content and encode the received content into at least two different protocols (col. 11, lines 30-61); and

a protocol select logic module (851F & 851S) that receives the content and forwards it to one of the at least two protocol encoder logic modules (col. 11, lines 30-45).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumaiya A. Chowdhury whose telephone number is (571) 272-8567. The examiner can normally be reached on Mon-Fri, 9-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SAC

  
ANDREW Y. KOENIG  
PRIMARY PATENT EXAMINER